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# A Structure-Reconfigurable Series Resonant DC-DC Converter With Wide-Input and Configurable-Output Voltages

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***Abstract*—This paper proposes a new series resonant DC-DC converter with four configurable operation states depending on the input voltage and output voltage levels. It suits well for the DC-DC stage of grid-connected photovoltaic (PV) systems with a wide-input voltage range and different grid voltage levels, i.e., 110/120 V and 220/230/240 V. The proposed converter consists of a dual-bridge structure on the primary side and a configurable half- or full-bridge rectifier on the secondary side. The root-mean-square (RMS) currents are kept low over a fourfold voltage-gain range; The primary-side MOSFETs and secondary-side diodes can achieve zero-voltage switching (ZVS) on and zero-current switching (ZCS) off, respectively. Therefore, the converter can maintain high efficiencies over a wide voltage gain range. A fixed-frequency pulse width modulated (PWM) control scheme is applied to the proposed converter, which makes the gain characteristics independent of the magnetizing inductance and thereby simplifies the design optimization of the resonant tank. The converter topology and operation principle are first described. Then the characteristics, i.e., the dc voltage gain, soft-switching, and RMS currents, are detailed before a performance comparison with conventional resonant topologies is carried out. Furthermore, the design guidelines of the proposed converter are also presented. Finally, the experimental results from a 500-W converter prototype verify feasibility of the proposed converter.**

***Index terms*—DC-DC converter, series resonant converter, reconfigurable structure, wide input voltage range, configurable output voltage.**

## I. INTRODUCTION

The deployment of renewable energies, e.g., photovoltaic (PV) and fuel cell, are becoming increasingly popular around the worldwide. For instance, in 2016, the growth in solar PV capacity was larger than any other form of generation; since 2010, costs of new solar PV have come down by 70% [1].

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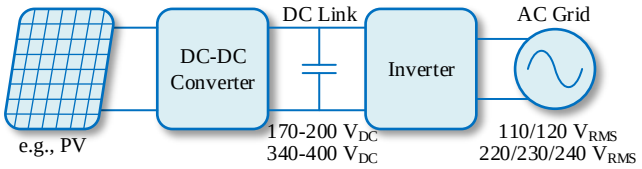



Fig. 1. Structure of a two-stage grid-connected renewable energy system [2]-[5].

In the literature, many different power conversion structures can be found for the grid-connected renewable system, e.g., the single-stage conversion, the two-stage conversion with a pseudo dc-link, and the two-stage conversion [2]-[5]. Fig. 1 shows the typical structure of a two-stage grid-connected renewable energy system [2]-[5]. Conventionally, the galvanic isolation between the renewable energy source and the grid is achieved by placing a bulky line-frequency transformer at the output of the inverter. In medium and low power applications, it has become a trend to include the isolation transformer in the high-frequency dc-dc stage or inverter stage. Thus, the isolation transformer volume can be shrunk significantly, and it can also help to eliminate the leakage current of PV panels [3], [4].

Renewable energy sources, e.g., PV and fuel cell, feature a wide range of output voltage. Thus, the interface dc-dc converter should be capable of maintaining high efficiency over a wide input voltage range [6]-[7]. Meanwhile, there are two different mains voltage levels, e.g., 110 V/120 V and 220 V/ 230 V/240 V, in different countries [8]. When connecting to a 220/230/240-V grid, the inverter typically has a dc-link voltage of 340-400 V. However, for a 110/120-V grid, it is preferable that the dc-link voltage is halved, i.e., 170-200 V; this way, the reduced voltage and increased modulation index could help to minimize the switching loss and output current harmonics of the inverter [9], [10]. Therefore, the dc-dc converter should also be able to configure its output voltage flexibly, e.g., either 340-400 V or 170-200 V.

Traditional forward/flyback converters with snubbers are simple in topology, but the voltage stress of the primary switches is high and thus low-voltage MOSFETs with low on-resistances cannot be used [6], [11], [12]. In the phase-shift full-bridge dc-dc converter, the primary switches can achieve zero-voltage-switching (ZVS); however, it suffers from great challenges when operating in a wide voltage gain range, e.g., the narrow ZVS range for the lagging leg switches, duty cycle

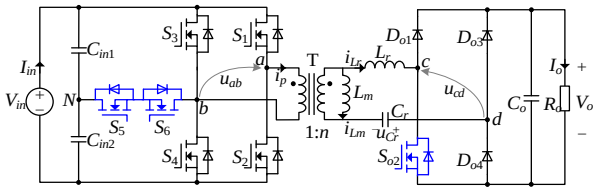



Fig. 2. Schematic of the proposed series resonant dc-dc converter.

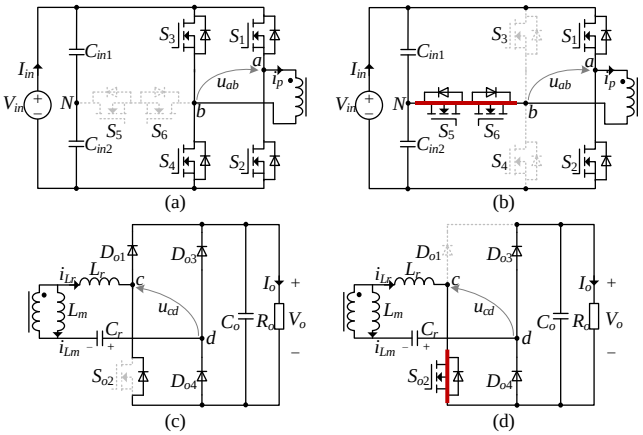



Fig. 3. Four structures in the proposed converter: (a) full-bridge inverter unit on the primary side; (b) symmetrical half-bridge inverter unit on the primary side; (c) full-bridge rectifier unit on the secondary side; (d) asymmetrical half-bridge rectifier (voltage doubler) unit on the secondary side.

loss, large circulating current, and voltage spikes across the output diodes [13], [14].

The LLC resonant converter has been widely adopted by industries due to its excellent performance in efficiency and power density [15]-[17]. Nevertheless, it is not able to handle a wide range of input voltage; otherwise, the switching frequency variation will be considerably large, and the transformer size and the conduction loss will increase significantly [18], [19]. In order to extend the input voltage range, many hybrid control schemes and resonant circuit topologies have been proposed [20]-[24]. In [20], a hybrid control combining the pulse-frequency modulation (PFM) and phase-shift pulse-width modulation (PS-PWM) is employed to the full-bridge LLC resonant converter; the efficiency performance is improved over a wide input range, but the control complexity is increased significantly as well. In [21], the bidirectional switch is added to the secondary resonant tank of a full-bridge series resonant dc-dc converter, whereas in [22], a bidirectional switch is placed on the primary side to form a dual-bridge LLC resonant converter. The full-bridge diode rectifier of resonant converters is replaced with a semi-active rectifier in [23]-[24]. All the modified topologies can deal with a wide range of input voltage while maintaining high efficiency; however, it is still difficult to configure their output voltage over a wide range.

Thanks to the electric vehicle industry boom, an increasing number of wide-output dc-dc converters emerge for battery chargers [25]-[30]. Most of the topologies are modified LLC resonant converter by altering the structures of the resonant tank [27], [28] or the output rectifier [29], [30]. This way, high efficiencies can be maintained over a wide output voltage range. However, the input voltages in [25]-[30] are fixed, and these topologies may not maintain high efficiencies when dealing with both wide-input and wide-output voltages.

The main contribution of this paper is that a structure-reconfigurable series resonant dc-dc converter which enables wide-input and configurable-output voltages, is proposed [31]. Both the primary-side inverter unit and secondary-side rectifier unit have two structures, and thus four structure combinations can be obtained. The reconfigurability enables the proposed converter with a fixed-frequency pulse-width modulation (PWM) scheme to achieve low conduction losses over a fourfold voltage gain range (from 0.5 to 2). Moreover, the primary switches and secondary switches/diodes can achieve ZVS-on and zero-current-switching (ZCS) off, respectively. As a result, this converter is able to maintain high efficiencies over a wide input voltage range and at two configurable output voltages. The proposed structure-reconfigurable SRC can be a good candidate for both 110/120-V and 220/230/240-V grid-connected renewable energy systems.

## II. Operation Principle of the Proposed Converter

### A. Topology and Operation Modes

The proposed universal series resonant dc-dc converter is shown in Fig. 2 [31]. Compared with the conventional full-bridge series resonant converter, two low-voltage switches $S_5$ and $S_6$ are inserted between the midpoints $N$ and $b$, and the rectifier diode $D_{o2}$ is replaced with a low-frequency switch $S_{o2}$. The voltage stress of $S_5$ and $S_6$ is only half of the input voltage, i.e., $V_{in}/2$.

There are four configurable structures in the proposed converter, as illustrated in Fig. 3. When $S_5$ and $S_6$ are turned off, the primary-side switches $S_1$–$S_4$ form a full-bridge inverter unit; when $S_5$ and $S_6$ are kept on and $S_3$ and $S_4$ are turned off, the two switches $S_1$–$S_2$ and the input capacitor $C_{in1}$–$C_{in2}$ constitute a symmetric half-bridge inverter unit on the primary side. Thus, the amplitude of the voltage across the primary transformer winding, $u_{ab}$, can be multi-level, i.e., $\pm V_{in}$, $\pm V_{in}/2$ and 0. For the proposed converter, the magnetizing current is used to charge/discharge the parasitic capacitances of primary-side MOSFETs such that a complete ZVS-on can be achieved. To avoid an over-low peak magnetizing current and an incomplete ZVS-on, the voltage level of $u_{ab}$ being 0 is not preferable. Thus, a two-level ($\pm V_{in}$ and $\pm V_{in}/2$) resonant tank voltage $u_{ab}$ is generated by adopting a fixed-frequency PWM scheme, as illustrated in Fig. 4. With this modulation, both the full-bridge inverter state and the symmetrical half-bridge inverter state occur on the primary side during each half switching cycle (see Fig. 4).

With regard to the secondary-side structures, when $S_{o2}$ is turned off, a full-bridge rectifier occurs and the output voltage $V_o$ is equal to the amplitude of $u_{cd}$; however, when $S_{o2}$ is kept in the on state, an asymmetrical half-bridge rectifier, i.e., a voltage doubler, can be formed and thus, the output voltage $V_o$ is double of the AC amplitude of $u_{cd}$. This implies that a low-voltage (LV) or high-voltage (HV) output can be configured flexibly by turning off or turning on $S_{o2}$. Therefore, the two operation states are termed as the LV output mode and HV output mode, respectively.

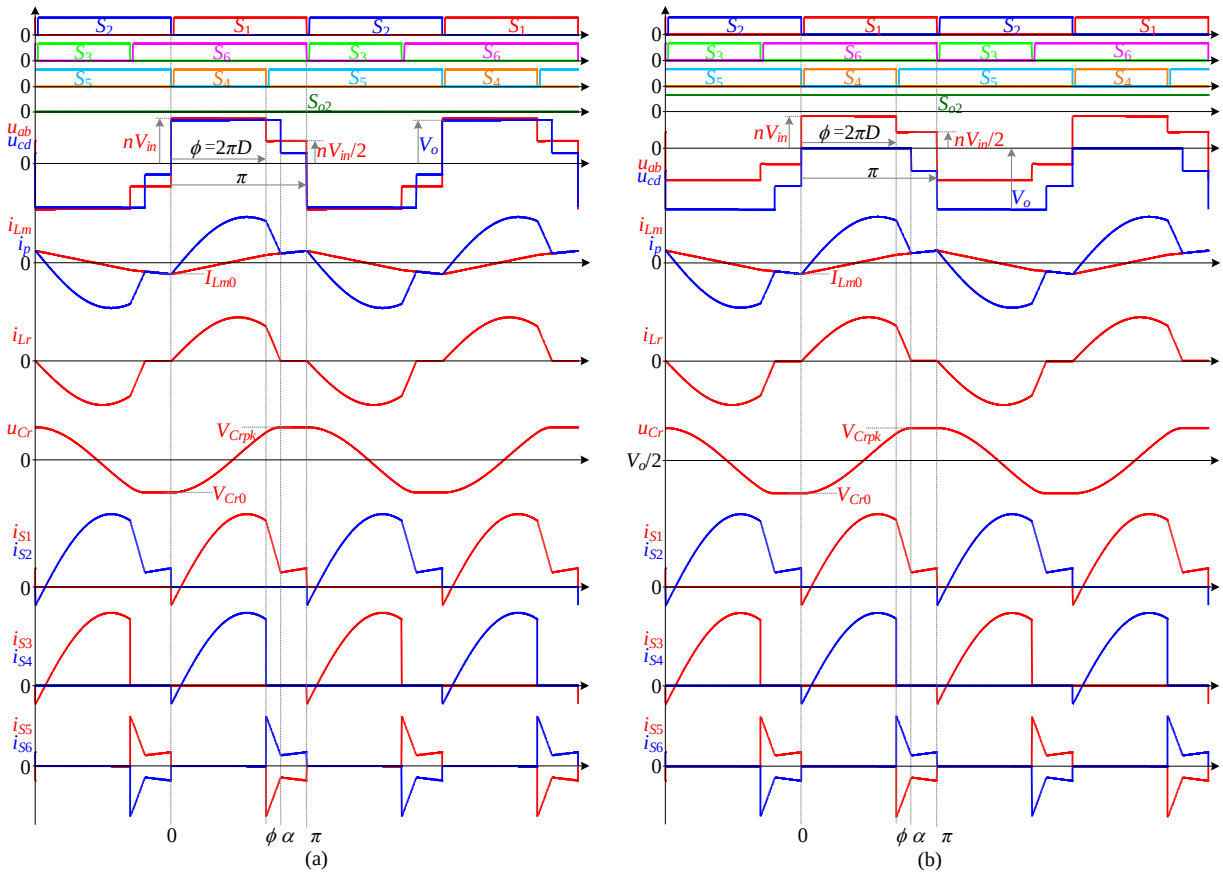



Fig. 4. Key waveforms of the converter operating in (a) the low-voltage (LV) output mode and (b) high-voltage (HV) output mode, where the output rectifier unit is configured as a full-bridge rectifier and an asymmetrical half-bridge rectifier (voltage doubler), respectively.

The key waveforms of the proposed converter in the two operation modes are shown in Fig. 4. It can be noticed that the main difference between the two operation modes lies in the two voltage waveforms $u_{cd}$ and $u_{Cr}$. In comparison with the LV output mode, there is a voltage offset of $V_o/2$ for $u_{Cr}$ and $u_o$ in the HV output mode. The output voltage in the HV output mode is double of that in the LV mode. Furthermore, both the current ripple frequency and amplitude of the output capacitor $C_o$ are halved in the HV output mode, leading to an equal output voltage ripple in both modes.

## B. Operation Principle

To simplify the analysis, the voltages and currents are normalized based on

$$\begin{cases} V_{base} = nV_{in} \\ I_{base} = nV_{in} / Z_r \end{cases} \tag{1}$$

where the characteristic impedance $Z_r = \sqrt{L_r / C_r}$.

The quality factor $Q$ is defined as

$$Q = \begin{cases} \dfrac{Z_r}{R_o} = \dfrac{P_o Z_r}{V_o^2}, & \text{LV output mode} \\ \dfrac{4Z_r}{R_o} = \dfrac{4P_o Z_r}{V_o^2}, & \text{HV output mode} \end{cases} \tag{2}$$

The voltage gain $G$ is defined as

$$G = V_o / (nV_{in}) \tag{3}$$

### 1) Low-Voltage Output Mode

In the LV output mode, the secondary-side switch $S_{o2}$ is kept off, but its anti-parallel diode $D_{o2}$ is used to form a full-bridge rectifier with other three output diodes $D_{o1}$, $D_{o3}$, $D_{o4}$. The voltage ripple across the resonant capacitor in this mode can be obtain by applying the ampere-second balance principle

$$\Delta V_{Cr} = \pi GQ \tag{4}$$

The initial resonant voltage equals to the valley voltage, i.e.,

$$V_{Cr0} = -\Delta V_{Cr} / 2 = -\pi GQ / 2 \tag{5}$$

Neglecting the deadtime, six stages can be identified over a switching cycle. Due to the symmetry of operation, only the first three stages over the first half switching cycle [0, $\pi$] are detailed.

***Stage I*** $\theta \in [0, \phi]$ (see Figs. 4(a) and 5(a)): $S_6$ has been conducting before $S_2$ and $S_5$ are turned off at $\theta = 0$. The negative magnetizing current $i_{Lm}$ begins to charge/discharge the output parasitic capacitors of $S_1$-$S_5$, i.e., $C_{oss1}$-$C_{oss5}$, such that $S_1$ and $S_4$ can achieve ZVS-on. At this stage, the voltage across the transformer, $u_{ab}$, equals to the input voltage $V_{in}$, and the inductor current $i_{Lr}$ rises sinusoidally from 0. The output diodes $D_{o1}$ and $D_{o4}$ are conducting, and the resonant tank voltage $u_{cd}$ equals to $V_o$. Thus, the normalized mathematic equations for the resonant tank can be expressed as

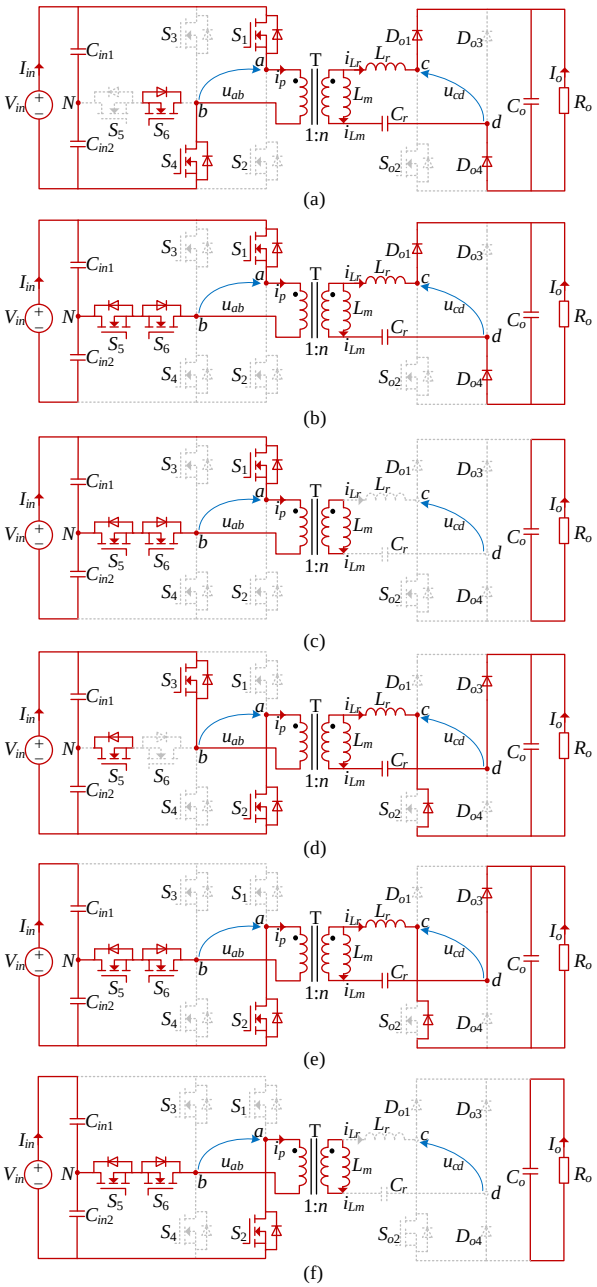



Fig. 5. Equivalent circuit of each switching state in the LV output mode: (a) Stage I [0, $\phi$]; (b) stage II [$\phi$, $\alpha$]; (c) stage III [$\alpha$, $\pi$]; (d) stage IV [$\pi$, $\pi$+$\phi$]; (e) stage V [$\pi$+$\phi$, $\pi$+$\alpha$]; (f) stage VI [$\pi$+$\alpha$, 2$\pi$].

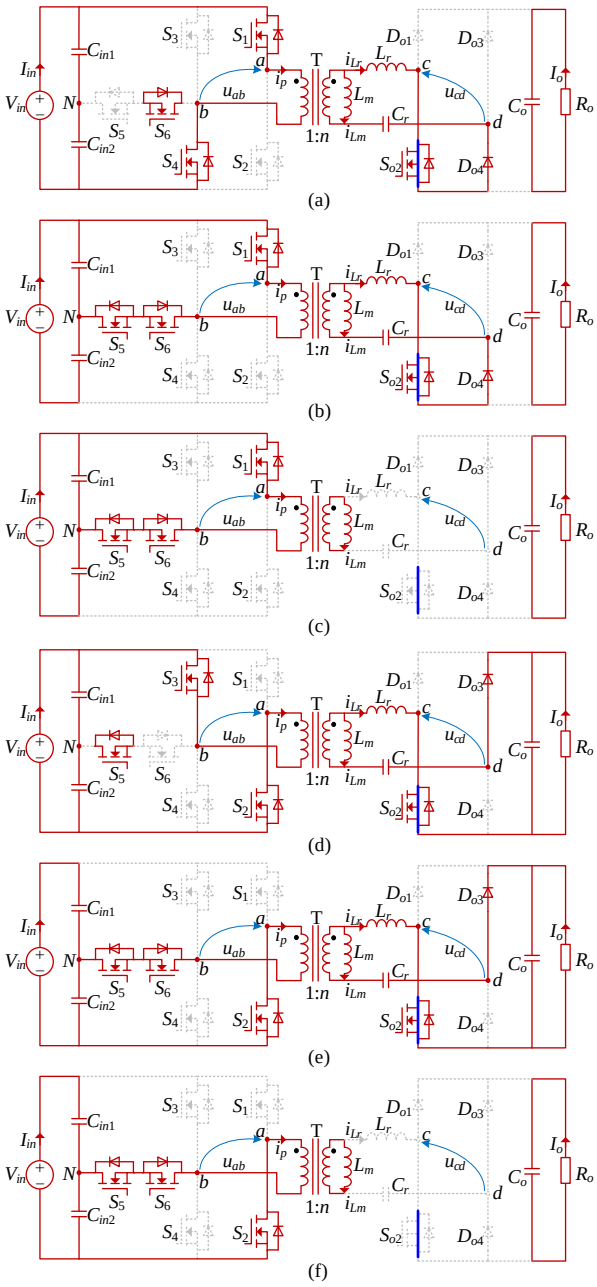



Fig. 6. Equivalent circuit of each switching state in the HV output mode: (a) Stage I [0, $\phi$]; (b) stage II [$\phi$, $\alpha$]; (c) stage III [$\alpha$, $\pi$]; (d) stage IV [$\pi$, $\pi$+$\phi$]; (e) stage V [$\pi$+$\phi$, $\pi$+$\alpha$]; (f) stage VI [$\pi$+$\alpha$, 2$\pi$];

$$\begin{cases} i_{Lr}(\theta) = r_1 \sin\theta \\ u_{Cr}(\theta) = 1 - G - r_1 \cos\theta \\ i_{Lm}(\theta) = I_{Lm0} + \theta \,/\, m \end{cases} \tag{6}$$

where $r_1 = 1 - G - V_{Cr0}$, and the inductors ratio $m = L_m \,/\, L_r$.

***Stage II*** $\theta \in [\phi, \alpha]$ (see Figs. 4(a) and 5(b)): At $\theta = \phi$, the switch $S_4$ is turned off, and thus the positive transformer current $i_p$ charges/discharges $C_{oss3}$-$C_{oss5}$ such that $S_5$ achieves ZVS. During this stage, the transformer voltage $u_{ab}$ equals to half of the input voltage, i.e., $u_{ab} = V_{in}/2$. Thus, the inductor current $i_{Lr}$ decreases sinusoidally. The output diodes $D_{o1}$ and $D_{o4}$ are still conducting, and the voltage $u_{cd}$ still equals to $V_o$. The normalized mathematic equations for the resonant tank can be expressed as

$$\begin{cases} i_{Lr}(\theta) = i_{Lr}(\phi)\cos(\theta-\phi) + r_2 \sin(\theta-\phi) \\ u_{Cr}(\theta) = i_{Lr}(\phi)\sin(\theta-\phi) - r_2 \cos(\theta-\phi) + 1/2 - G \\ i_{Lm}(\theta) = i_{Lm}(\phi) + \theta \,/\, (2m) \end{cases} \tag{7}$$

where $r_2 = 1/2 - G - V_{Cr}(\phi)$.

***Stage III*** $\theta \in [\alpha, \pi]$ (see Figs. 4(a) and 5(c)): The inductor current $i_{Lr}$ decreases to 0 at $\theta = \alpha$, and the rectifier diodes $D_{o1}$

and $D_{o4}$ turn off with ZCS. Due to the unidirectionality of diodes, reverse resonance is not possible. Thus, both the resonant inductor current and the resonant capacitor voltage are kept unchanged. However, the magnetizing inductor is excited by $u_{ab}$, and therefore $i_{Lm}$ increases linearly, i.e.,

$$\begin{cases} i_{Lr}(\theta) = i_{Lr}(\alpha) \\ u_{Cr}(\theta) = u_{Cr}(\alpha) \\ i_{Lm}(\theta) = i_{Lm}(\alpha) + \theta / (2m) \end{cases} \tag{8}$$

During all the operation stages, the primary transformer current $i_p$ can be always expressed as

$$i_p = i_{Lr} + i_{Lm} \tag{9}$$

*2) High-Voltage Output Mode*

In the HV output mode, the secondary-side switch $S_{o2}$ is kept in the on state. The voltage ripple across the resonant capacitor can be calculated as

$$\Delta V_{Cr} = \pi G Q / 2 \tag{10}$$

The voltage offset for the capacitor $V_{Cr\_dc}$ is half of the output voltage. Thus, its normalized initial resonant voltage is

$$V_{Cr0} = V_{Cr\_dc} - \Delta V_{Cr} / 2 = G / 2 - \pi G Q / 4 \tag{11}$$

Similarly, six stages are included during each switching cycle by neglecting the deadtime. Due to the symmetry of operation, only the first three stages over the first half switching cycle [0, $\pi$] are described. The primary-side switches operate in the same way as in the LV output mode; the only difference occurs on the secondary side which will be elaborated.

***Stage I*** $\theta \in [0, \phi]$ (see Figs. 4(b) and 6(a)): At this stage, $u_{ab}$ equals to $V_{in}$, $S_{o2}$ and $D_{o4}$ are conducting, and the voltage $u_{cd}$ equals to zero. Thus, the normalized mathematic equations for the resonant tank can be expressed as

$$\begin{cases} i_{Lr}(\theta) = \lambda_1 \sin\theta \\ u_{Cr}(\theta) = 1 - \lambda_1 \cos\theta \\ i_{Lm}(\theta) = I_{Lm0} + \theta / m \end{cases} \tag{12}$$

where $\lambda_1 = 1 - V_{Cr0}$.

***Stage II*** $\theta \in [\phi, \alpha]$ (see Figs. 4(b) and 6(b)): After $\theta = \phi$, $u_{ab}$ equals to $V_{in}/2$, $S_{o2}$ and $D_{o4}$ are still conducting, and the voltage $u_{cd}$ still equals to zero. The normalized mathematic equations for the resonant tank can be expressed as

$$\begin{cases} i_{Lr}(\theta) = i_{Lr}(\phi)\cos(\theta-\phi) + \lambda_2 \sin(\theta-\phi) \\ u_{Cr}(\theta) = i_{Lr}(\phi)\sin(\theta-\phi) - \lambda_2 \cos(\theta-\phi) + 1/2 \\ i_{Lm}(\theta) = i_{Lm}(\phi) + \theta / (2m) \end{cases} \tag{13}$$

where $\lambda_2 = 1/2 - V_{Cr}(\phi)$.

***Stage III*** $\theta \in [\alpha, \pi]$ (see Figs. 4(b) and 6(c)): At $\theta = \alpha$, the inductor current $i_{Lr}$ decreases to 0, and $D_{o4}$ turns off with ZCS. It results in

$$\begin{cases} i_{Lr}(\theta) = i_{Lr}(\alpha) \\ u_{Cr}(\theta) = u_{Cr}(\alpha) \\ i_{Lm}(\theta) = i_{Lm}(\alpha) + \theta / (2m) \end{cases} \tag{14}$$

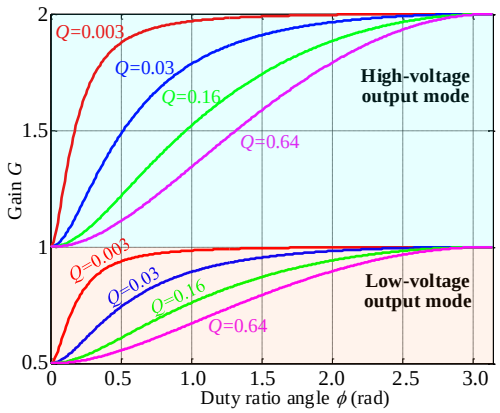



Fig. 7. Characteristics of the voltage gain with respect to the duty ratio angle $\phi$ and the quality factor $Q$ in the LV and HV output modes.

## III. Characteristics of the Proposed Converter

### A. DC Voltage Gain

The initial magnetizing current in both the HV and LV modes can be derived as

$$I_{Lm0} = -\frac{\pi + \phi}{4m} \tag{15}$$

By applying the odd symmetry of the resonant voltage and current to (6) – (14), the voltage gain $G$ can be obtained for both modes

$$G = \frac{3\pi Q - 2 + (2 - \pi Q)\cos\phi + K}{8\pi Q} \times \begin{cases} 1, \text{LV output mode} \\ 2, \text{HV output mode} \end{cases} \tag{16}$$

where $K = \sqrt{8\pi Q \sin^2\phi + [3\pi Q + 2 - (\pi Q + 2)\cos\phi]^2}$.

The curves of the voltage gain with respect to the duty ratio angle $\phi$ for different quality factors are shown in Fig. 7. As can be seen, the voltage gain range is from 0.5 to 2 regardless of the quality factor $Q$. In addition, it is seen that the dc voltage gain of the proposed converter is independent of the inductors ratio $m$, which is different from the conventional LLC resonant converter. Thus, the magnetizing inductance can be designed solely based on the ZVS conditions of MOSFETs.

In order to ensure the normal operation of the proposed converter, the peak voltage across the resonant capacitor, $V_{Crpk}$, cannot be higher than the output voltage $V_o$. Then the boundary conditions of normal operation can be obtained for both operation modes

$$Q \le \frac{2}{\pi} \Rightarrow \begin{cases} Z_r \le 2V_o^2 / (\pi P_o), \text{ LV output mode} \\ Z_r \le V_o^2 / (2\pi P_o), \text{ HV output mode} \end{cases} \tag{17}$$

Since the output voltage in the HV output mode is double of that in the LV output mode, the boundary conditions in (17) are the same for both modes.

### B. Root-Mean-Square Currents

The root-mean-square (RMS) currents flowing through $S_3/S_4$ and $S_5/S_6$ in both the LV and HV output mode are calculated by

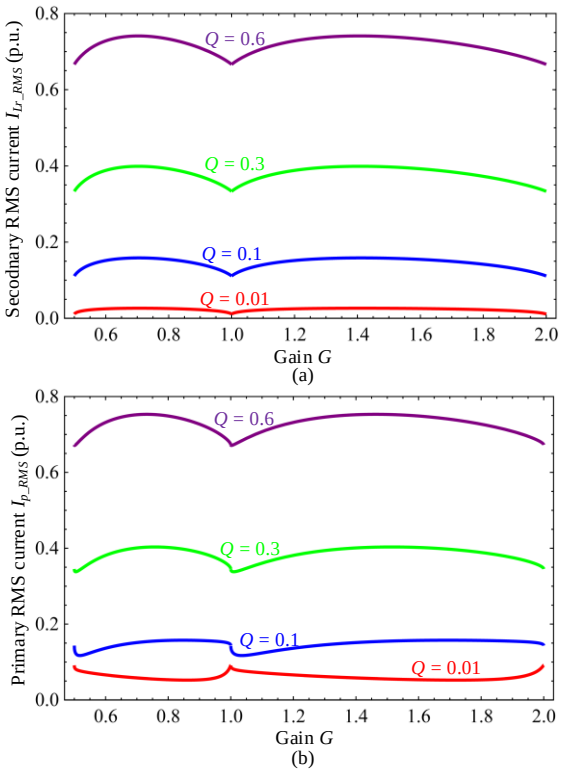



Fig. 8. The RMS currents with respect to the voltage gain $G$ and the quality factor $Q$. (a) Secondary transformer RMS current; (b) Primary transformer RMS current.

$$\begin{cases} I_{S34\_rms} = \sqrt{\dfrac{1}{2\pi}\int_0^{\phi} i_{Lp}^2(\theta)\,\mathrm{d}\theta} \\ \quad = \sqrt{\dfrac{\left\{\begin{array}{l} 6mI_{Lm0}[m\phi I_{Lm0} + 2mr(1-\cos\phi) + \phi^2] + 2\phi^3 \\ \quad + 3mr(mr\phi - [\sin\phi(mr\cos\phi - 4) + 4\phi\cos\phi])\end{array}\right.}{12\pi m^2}} \\ I_{S56\_rms} = \sqrt{\dfrac{1}{\pi}\int_{\phi}^{\pi} i_{Lp}^2(\theta)d\theta} \\ = \sqrt{\dfrac{3m\left\{\begin{array}{l} I_{Lm2}[4Am(1-\cos\delta) - \delta^2] + \delta I_{Lm0}(2mI_{Lm0} + \delta) \\ +2m\delta I_{Lm2}^2 + A[2\delta\cos\delta - \sin\delta(Am\cos\delta + 2) + Am\delta]\end{array}\right\} + \delta^3}{6\pi m^2}} \end{cases} \tag{18}$$

where $I_{Lm2} = i_{Lm}(\alpha)$, $\delta = \alpha - \phi$, and $A = \sqrt{i_{Lr}^2(\phi) + r_2^2}$.

Then the RMS currents flowing through the primary transformer winding and $S_3$/$S_4$ can be derived by

$$\begin{cases} I_{Lp\_rms} = \sqrt{2I_{S34\_rms}^2 + I_{S56\_rms}^2} \\ I_{S12\_rms} = I_{Lp\_rms} / \sqrt{2} \end{cases} \tag{19}$$

With regard to the resonant RMS current, it is obtained as

$$I_{Lr\_rms} = \sqrt{\frac{1}{\pi}\int_0^{\delta} i_{Lr}^2(\theta)\,\mathrm{d}\theta} = \sqrt{\frac{r_1^2[2\phi - \cos(2\phi)] + A^2[2\delta - \cos(2\delta)]}{4\pi}} \tag{20}$$

However, the mathematical expressions of the RMS currents flowing through $D_{o1}$ and $S_{o2}$ are different in the two modes:

$$\begin{cases} I_{Do1\_rms} = \begin{cases} I_{Lr\_rms}/\sqrt{2}, & \text{LV output mode} \\ 0, & \text{HV output mode} \end{cases} \\ I_{So2\_rms} = \begin{cases} I_{Lr\_rms}/\sqrt{2}, & \text{LV output mode} \\ I_{Lr\_rms}, & \text{HV output mode} \end{cases} \\ I_{Do34\_rms} = I_{Lr\_rms}/\sqrt{2}, \quad \text{Both modes} \end{cases} \tag{21}$$

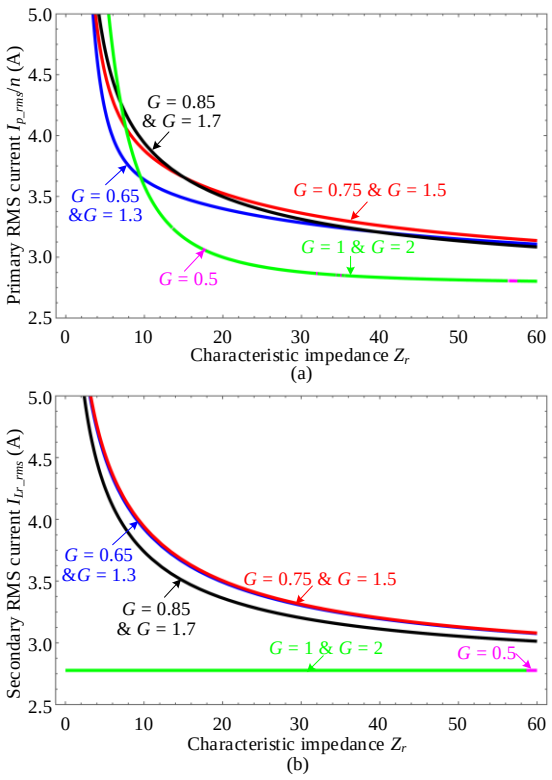



Fig. 9. Full-load RMS currents with respect to the characteristic impedance $Z_r$.

Based on (19) and (20), the curves of the primary and secondary transformer RMS currents $I_{p\_RMS}$ and $I_{Lr\_RMS}$ are plotted in Fig. 8. It can be seen that the variations of the two RMS currents with respect to the voltage gain $G$ are small. This means that the converter can achieve low conduction losses over the entire voltage gain range of [0.5, 2].

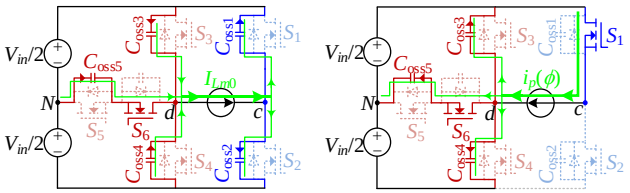
When the load is fixed, the relationship between the primary and secondary RMS currents and the characteristic impedance $Z_r$ can be obtained, as shown in Fig. 9 (at full load 500 W). The RMS currents drops with respect to the increase of $Z_r$ except for the three special cases $G$ = 0.5, 1, and 2 in Fig. 9(b). In order to decrease the conduction losses, the characteristic impedance $Z_r$ should be designed possibly large under the premise of the boundary conditions in (17).

### C. Soft-Switching

As aforementioned, the primary-side switches $S_1$-$S_6$ can achieve ZVS-on. In practice, however, the realization of ZVS-on requires sufficient charges to completely charge/discharge the parasitic output capacitances of power MOSFETs $S_1$-$S_6$. Since the operation of the primary-side inverter unit remains the same for both the LV and HV output modes, the ZVS characteristics in the LV output mode will be analyzed. Also, due to the symmetry of circuit and modulation, only the commutations during the half switching cycle $\theta \in [0, \pi]$ are analyzed, as shown in Fig. 10. In order to quantify the required amount of charges for each commutation mode, detailed state analysis for the half switching cycle $\theta \in [0, \pi]$ is presented in Table I, where $C_{oss14}$ denotes the output capacitance of $S_1$-$S_2$, and $C_{oss56}$ represents the output capacitance of $S_5$-$S_6$.

TABLE I
REQUIRED MINIMUM CHARGE TO ACHIEVE ZVS FOR DIFFERENT SWITCH LEGS

| Commutation mode | Current to achieve ZVS | Charged/dis-charged capacitor | | Initial voltage | Final voltage | Absolute charge variation of a capacitor | Charge variation of a HB/T-type leg | Minimum charge $q_{req}$ for ZVS-ON of all switches |
|---|---|---|---|---|---|---|---|---|
| ZVS-on of $S_1$ and $S_4$ (see Figs. 4 and 11(a)) | $I_{Lm0}$ | HB leg | $C_{oss1}$ | $V_{in}$ | 0 | $V_{in}C_{oss14}$ | $2V_{in}C_{oss14}$ | $q_{reqI}$ = **max{$2V_{in}C_{oss14}$, $V_{in}(C_{oss14}+0.5C_{oss56})$}** |
| | | | $C_{oss2}$ | 0 | $V_{in}$ | $V_{in}C_{oss14}$ | | |
| | | T-type leg | $C_{oss3}$ | $0.5V_{in}$ | $V_{in}$ | $0.5V_{in}C_{oss14}$ | $V_{in}(C_{oss14}+0.5C_{oss56})$ | |
| | | | $C_{oss4}$ | $0.5V_{in}$ | 0 | $0.5V_{in}C_{oss14}$ | | |
| | | | $C_{oss5}$ | 0 | $0.5V_{in}$ | $0.5V_{in}C_{oss56}$ | | |
| | | | $C_{oss6}$ | 0 | 0 | 0 | | |
| ZVS-on of $S_5$ (see Figs. 4 and 11(b)) | $i_p(\phi)$ | HB leg | $C_{oss1}$ | 0 | 0 | 0 | 0 | $q_{reqII}$ = $V_{in}(C_{oss14}+0.5C_{oss56})$ |
| | | | $C_{oss2}$ | $V_{in}$ | $V_{in}$ | 0 | | |
| | | T-type leg | $C_{oss3}$ | $V_{in}$ | $0.5V_{in}$ | $0.5V_{in}C_{oss14}$ | $V_{in}(C_{oss14}+0.5C_{oss56})$ | |
| | | | $C_{oss4}$ | 0 | $0.5V_{in}$ | $0.5V_{in}C_{oss14}$ | | |
| | | | $C_{oss5}$ | $0.5V_{in}$ | 0 | $0.5V_{in}C_{oss56}$ | | |
| | | | $C_{oss6}$ | 0 | 0 | 0 | | |




(a) (b)

Fig. 10. ZVS mechanism of primary-side switches. (a) ZVS-on of $S_1$ and $S_4$ at $t = 0$ (see Fig.4), (b) ZVS-on of $S_5$ at $t = \phi/\omega_r$ (i.e., $\theta = \phi$, see Fig. 4).

The ZVS-on of $S_1$/$S_4$ and $S_5$ depends on the currents $I_{Lm0}$ and $i_p(\phi)$, respectively. The inductors ratio $m$ has a direct impact on the peak magnetizing current $I_{Lm0}$ (15), and therefore determines the ZVS realizations of $S_1$-$S_4$. The current $I_{Lm0}$ can be assumed to be constant during the deadtime interval $t_d$ which is short compared to the switching period.

In order to achieve the ZVS-on of $S_1$-$S_4$, sufficient charge should be provided during the deadtime interval, i.e.,

$$\left|nI_{base}I_{Lm0}\right|t_d = -nI_{base}I_{Lm0}t_d > q_{reqI} \tag{22}$$

Combining (15), (22) and Table I yields the selection criterion for the magnetizing inductance $L_m$

$$L_m < \frac{t_d n^2 V_{in}(\pi+\phi)}{8\pi q_{reqIII} f_r} \tag{23}$$

where $\phi = \arccos\left(\frac{G[\pi Q(3-4G)-2]+2}{G(\pi Q-2)+2}\right)$.

As illustrated in Table I, the ZVS realization of $S_5$ and $S_6$ relies on the currents $i_p(\phi)$ which can be expressed as

$$i_p(\phi) = \frac{n^2 V_{in}}{Z_r}\left(I_{Lm0} + \phi/m + r_1\sin\phi\right) \tag{24}$$

The ZVS condition of $S_5$ and $S_6$ can be derived as

$$\begin{aligned} & i_p(\phi)t_d \geq q_{reqII} \\ & \Rightarrow Q \geq \frac{4mZ_r q_{reqII} + n^2 t_d V_{in}(\pi-3\phi)}{2\pi G m n^2 t_d V_{in}\sin\phi} - \frac{2(1-G)}{\pi G} \end{aligned} \tag{25}$$

Based on (25), the soft- and hard-switching areas of $S_5$ and $S_6$ can be obtained, as shown in Fig. 11. It's seen that the hard-switching area is small compared with the soft-switching area.

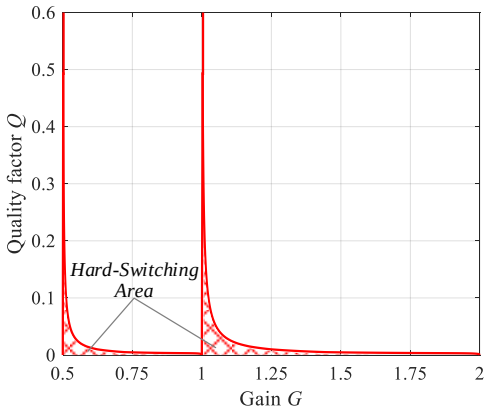



Fig. 11. Soft- and hard-switching areas of $S_5$ and $S_6$. The filled area represents the hard-switching range, whereas the rest represents the soft-switching area.

## D. Performance Comparison

The voltage gain characteristics of the conventional full-bridge SRC and LLC resonant converter are shown in Fig. 12. For the pulse-frequency-modulated (PFM) SRC, the light-load gain range is narrow even within a wide normalized switching frequency range $f_n \in [1, 5]$, as indicated in Fig. 12(a). The PFM LLC resonant converter has an improved gain characteristics. However, the heavy-load gain range is still narrow (see Fig. 12(b)). In order to have a high full-load voltage gain peak, the characteristic impedance has to be decreased, thereby resulting in a wide frequency range and/or high magnetizing current and conduction losses [18], [19], [28]-[30].

With the fixed-frequency PWM or phase-shift modulation (PSM) control, the gain ranges of the conventional SRC and LLC resonant converter are extended, as shown in Figs. 12(c) and (d). However, the main issue is that the duty cycle variation is wide. When the duty cycle $D$ is small, the conduction losses will rise and the soft-switching condition will be lost because the magnetizing current is reduced significantly in this case, as illustrated in Fig. 13. By contrast, both the RMS current and the magnetizing current of the proposed resonant converter do not vary significantly with respect to the gain $G$, as illustrated in Figs. 8 and 13. Thus, the ZVS-on of MOSFETs can be achieved and the conduction losses can be maintained low within a wide voltage gain range [0.5, 2]. Furthermore, the voltage gain range

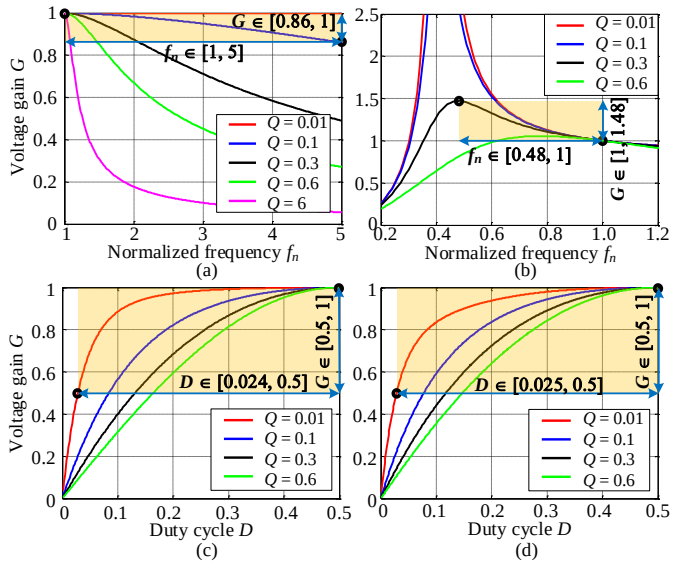



Fig. 12. Voltage gain characteristics of the conventional full-bridge SRC and LLC resonant converter. (a) SRC with PFM control; (b) LLC resonant converter with PFM control; (c) SRC with PWM or PSM control; (d) LLC resonant converter with PWM or PSM control.

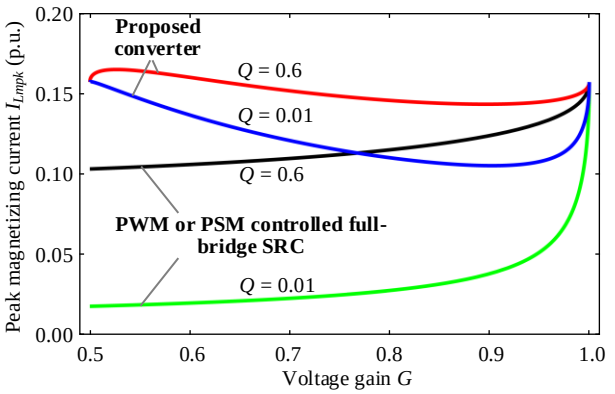



Fig. 13. Peak magnetizing currents with respect to the voltage gain $G$ for the proposed converter and the conventional full-bridge series resonant converter.

TABLE II
CONVERTER PARAMETERS

| Description | Symbol | Parameter |
|---|---|---|
| Input voltage | $V_{in}$ | 30–60 V |
| Output voltage | $V_o$ | 200/400 V |
| Switching frequency | $f_s$ | 100 kHz |
| Rated power | $P_o$ | 500 W |
| Primary switches | $S_1$–$S_4$ | IPP023N10N5, TO220 |
| | $S_5$–$S_6$ | IPP020N06N, TO220 |
| Secondary diodes/switch | $D_{o1}$, $D_{o3}$, $D_{o4}$ | STTH3R06, DO201 |
| | $S_{o2}$ | IPW65R110CFD, TO247 |
| Transformer | T | Turns ratio: 4 : 27<br>Magnetizing inductance $L_m$ = 450 μH. |
| Resonant Inductor | $L_r$ | 38.4 μH |
| Resonant capacitor | $C_r$ | 66 nF |

of the proposed converter is independent of the inductors ratio $m$, i.e., the magnetizing inductance $L_m$ does not affect the voltage tage gain $G$. Hence, the design of $L_m$ and the resonant tank ($L_r$ and $C_r$) can be carried out separately, which is easier than the conventional LLC resonant converter.

### E. Design Guideline

Considering the voltage gain range of [0.5, 2] (see Fig. 7) and the specified input and output voltage ranges (e.g., $V_{in}$ ∈ [30 V, 60 V] and $V_o$ = 200/400 V), the transformer turns ratio can be determined by

$$n = N_s : N_p = \frac{V_o}{GV_{in}} = 6.67 \tag{26}$$

In practice, $n$ = 27 : 4 = 6.75 is designed for the transformer.

Unlike the conventional LLC resonant converters, the voltage gain of the proposed converter is independent of the inductors ratio $m$, and thus, the design of the resonant tank ($L_r$ and $C_r$) and the magnetizing inductance $L_m$ can be performed separately. As analyzed in Section III-B, the transformer RMS currents decreases with respect to the increase of the characteristic impedance $Z_r$ at a specific load. In order to reduce the conduction losses, $Z_r$ should be designed possibly large on the premise of (17). On the other hand, it is seen from Fig. 9 that the RMS current curves become flat when $Z_r$ exceeds a certain value. However, a large $Z_r$ will lead to a high voltage ripple for the resonant capacitor. Therefore, a trade off should be considered in practice. Nevertheless, the design of $L_r$ and $C_r$ should follow

$$\begin{cases} f_s = \dfrac{1}{2\pi\sqrt{L_r C_r}} \\ Z_r = \sqrt{\dfrac{L_r}{C_r}} \le \min\left(\dfrac{2V_{o,LV}^2}{\pi P_{o,\max}}, \dfrac{V_{o,HV}^2}{2\pi P_{o,\max}}\right) \end{cases} \tag{27}$$

where $P_{o,max}$ is the maximum output power, $V_{o,LV}$ and $V_{o,HV}$ represent the output voltages in the LV and HV output modes. In this paper, the switching frequency $f_s$ = 100 kHz, $P_{o,max}$ = 500 W, $V_{o,LV}$ = 200 V and $V_{o,HV}$ = 400 V. Substituting the specifications to (27) and considering the availability of discrete resonant capacitors yield $L_r$ = 38.4 μH and $C_r$ = 66 nF.

As aforementioned, the magnetizing inductance affects the ZVS conditions of primary-side switches. A smaller magnetizing inductance facilitates the ZVS realization of $S_1$-$S_4$, but it also results in a larger magnetizing (circuiting) current, and higher conduction losses. Therefore, the magnetizing inductance should be designed possibly large under the condition of satisfying the ZVS condition (23).

## IV. EXPERIMENTAL VERIFICATIONS

A 500-W converter prototype has been built and its specifications and key parameters are listed in Table II. The full-load (500-W) experimental waveforms of the proposed converter in the LV ($V_o$ = 200 V) and HV ($V_o$ = 400 V) output modes are shown in Figs. 14 and 15, respectively. As can be seen, the steady-state operation matches well with the analysis. The proposed converter can deal with a wide input voltage range (from 30 V to 60 V) in both LV and HV output modes by changing the duty ratio angle $\phi$. When the input voltage is between the range of (30 V, 60 V), e.g., $V_{in}$ = 40 V in Figs. 14(b) and 15(b) and $V_{in}$ = 50 V in Figs. 14(c) and 15(c), both the full-bridge and half-bridge states appear on the primary-side inverter unit. In both the LV and HV output modes, the primary-side switches operate in the same way, leading to the same

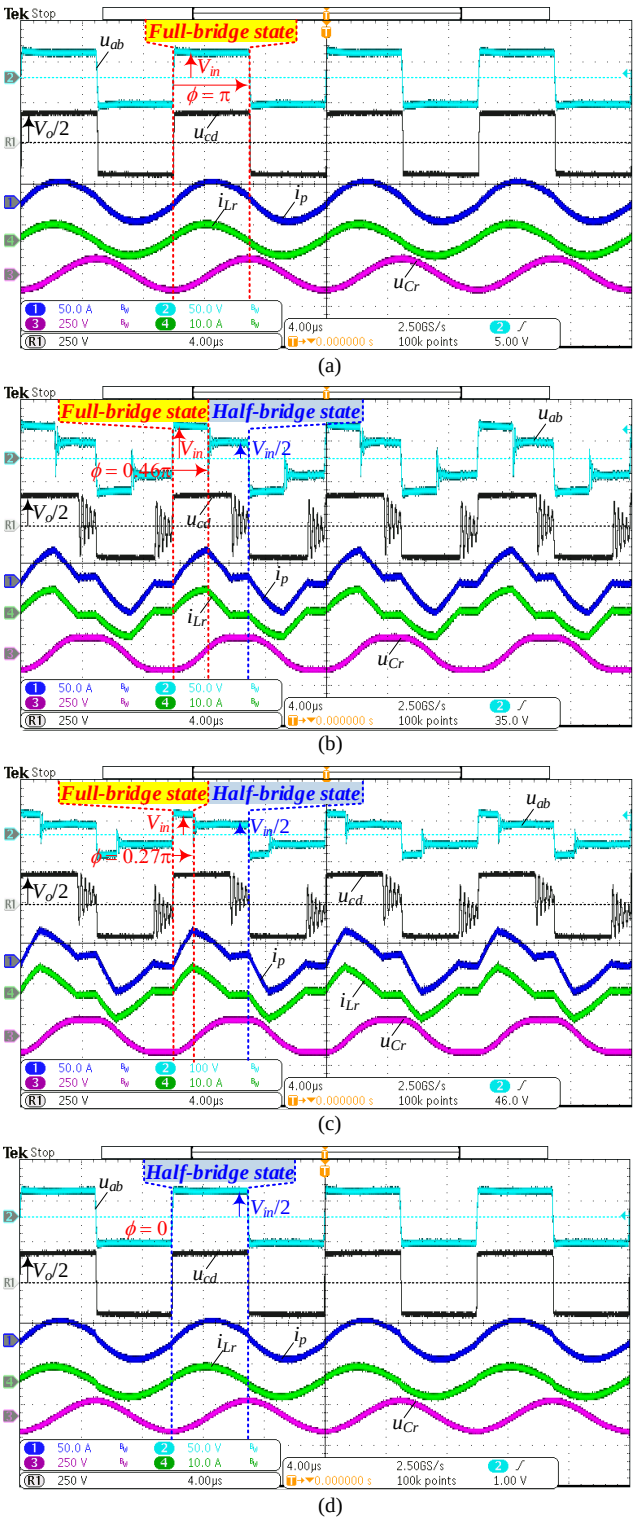



Fig. 14. Full-load experimental waveforms when operating in the LV output mode, i.e., $V_o$ = 200 V. (a) $V_{in}$ = 30 V; (b) $V_{in}$ = 40 V; (c) $V_{in}$ = 50 V; (d) $V_{in}$ = 60 V.

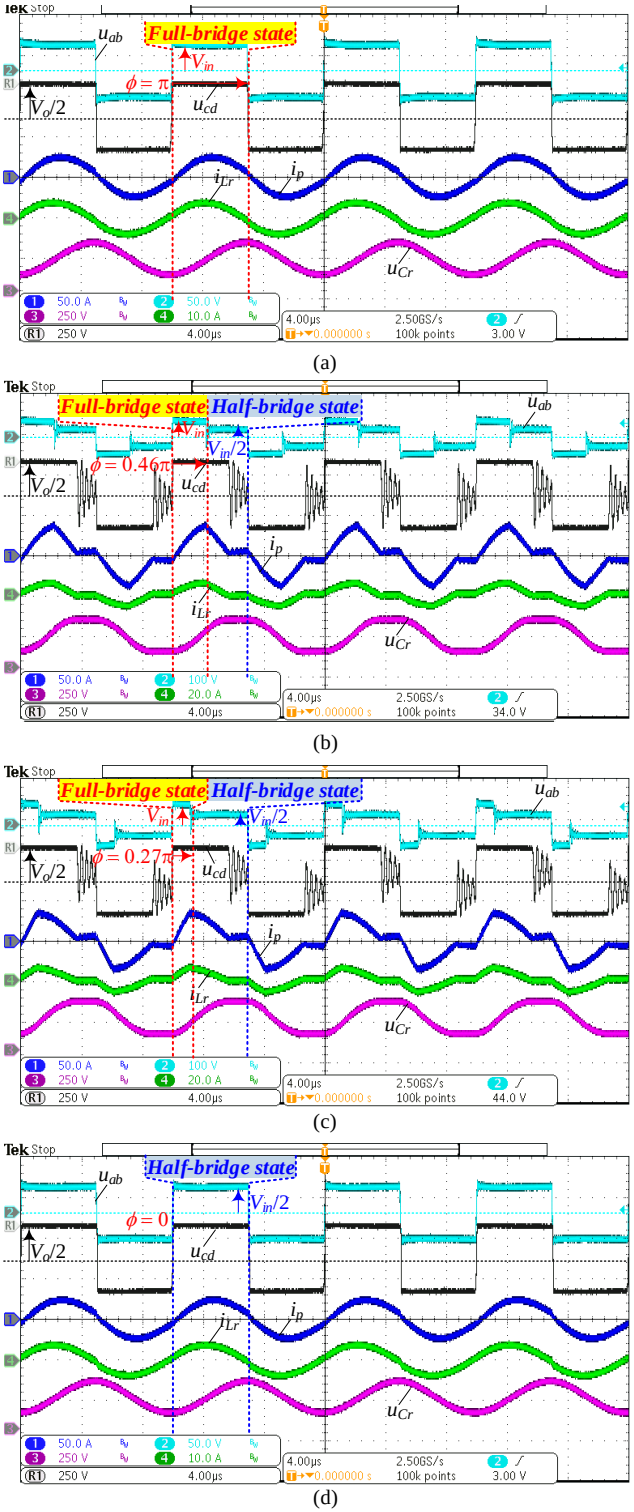



Fig. 15. Full-load experimental waveforms when operating in the HV output mode, i.e., $V_o$ = 400 V. (a) $V_{in}$ = 30 V; (b) $V_{in}$ = 40 V; (c) $V_{in}$ = 50 V; (d) $V_{in}$ = 60 V.

current waveforms. However, the resonant voltage waveforms are different in both modes: $u_{Cr}$ has a dc offset of 200 V in the HV output mode, whereas the offset in the LV output mode is zero. In addition, it can be noticed that there are high-frequency oscillations in $u_{cd}$ when the resonant current $i_{Lr}$ is in the discontinuous mode. The ringing is caused by the resonance between the resonant inductor $L_r$ and the resonant capacitor $C_r$ in series with the parasitic capacitors (e.g., the intra-winding capacitance of transformer, output capacitance of rectifier diodes, and stray capacitance of printed circuit board traces).

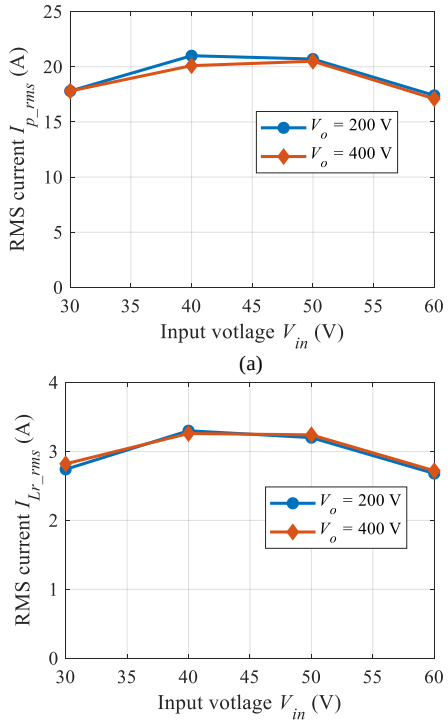



Fig. 16. Measured transformer RMS currents of the proposed converter at full-load (500-W) for different input and output voltages. (a) Transformer primary-side RMS current; (b) transformer secondary-side RMS current.

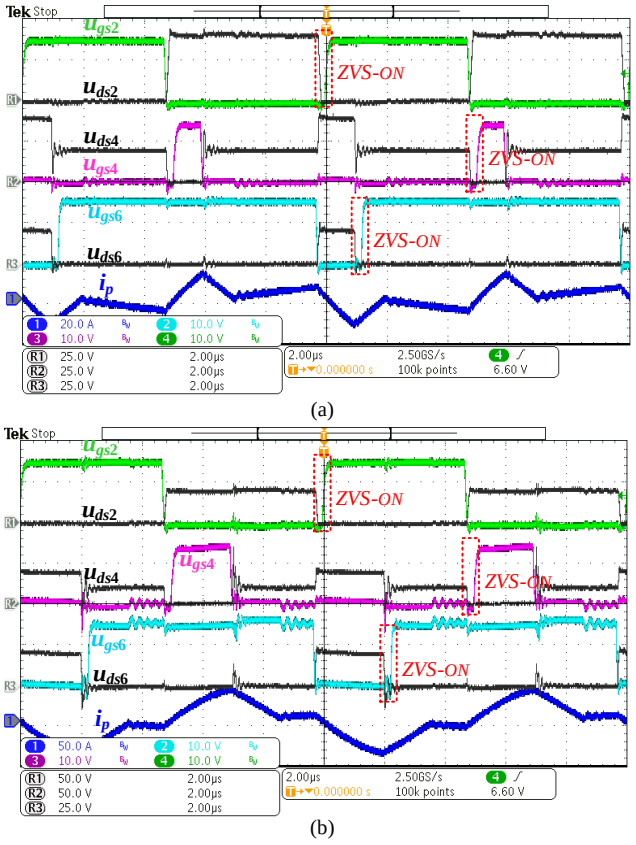



Fig. 17. Soft-switching waveforms in different operating conditions. (a) $V_{in}$ = 40 V, $V_o$ = 400 V, $P$ = 100 W; (b) $V_{in}$ = 40 V, $V_o$ = 400 V, $P$ = 500 W.

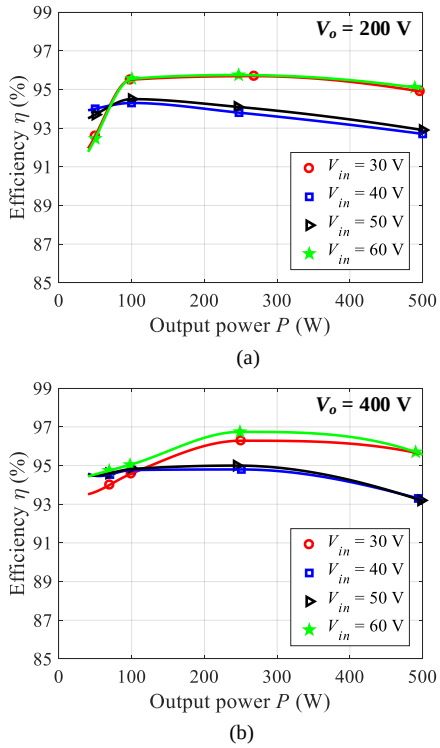



Fig. 18. Efficiency with respect to the output power for different input and output voltages (a) $V_o$ = 200 V; (b) $V_o$ = 400 V.

The measured transformer RMS currents at different input and output voltages are shown in Fig. 16. As can be seen, the RMS currents do not vary significantly with respect to the input voltage. Thus, the conduction loss can be kept low over the entire voltage gain range.

The soft-switching waveforms are shown in Fig. 17. Due to the symmetry of topology and operation, the drain-source and gate driver voltages of $S_2$, $S_4$ and $S_6$ are given. As can be seen, the drain-source voltage has decreased to zero before the corresponding gate driver voltage applies, implying the ZVS-on is achieved for MOSFETs.

The efficiency performance of the proposed converter is measured under different conditions, as shown in Fig. 18. It indicates that a high-efficiency power conversion can be achieved over the wide voltage gain range from 0.5 to 2. Depending on the input voltage $V_{in}$, the measured full-load efficiency varies between 92.8 % and 95.4 % for the two output-voltage cases $V_o$ = 200 V and $V_o$ = 400 V. Notably, the efficiency performance at $V_{in}$ = 40 V and $V_{in}$ = 50 V is deteriorated compared with that at $V_{in}$ = 30 V and $V_{in}$ = 60 V.

A power loss breakdown of the proposed converter is performed at different input and output voltages, as shown in Fig. 19. It is seen that the power semiconductor devices and magnetic components are the main power loss sources. The power loss distribution in the two cases $V_o$ = 200 V and $V_o$ = 400 V are almost the same except for $D_{o1}$ and $S_{o2}$. Therefore, the measured full-load efficiencies at $V_o$ = 200 V and $V_o$ = 400 V are close in Figs. 18(a) and (b). However, as the change of the input voltage $V_{in}$, e.g., $V_{in}$ deviates from 30 V and 60 V, the conduction losses of components become higher. Notably, the

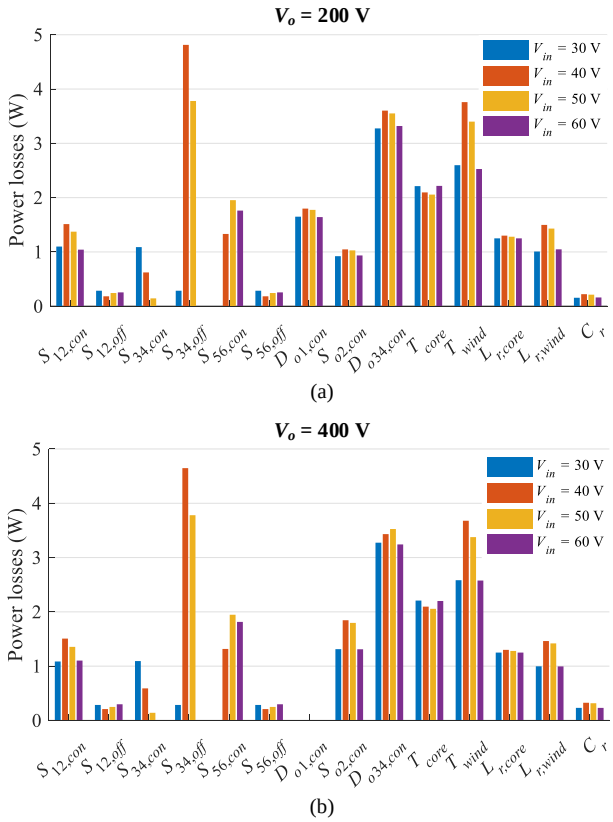



Fig. 19. Power loss breakdown at different input and output voltages (a) $V_o$ = 200 V; (b) $V_o$ = 400 V.

off-switching losses of $S_3$ and $S_4$ are significantly increased at $V_{in}$ = 40 V and $V_{in}$ = 50 V, which results in the measured efficiency drop in Figs. 18(a) and (b).

The issue of high off-switching losses can be alleviated by taking the following precautions:

1) minimize the loop inductance by introducing the capacitive layout [32] and/or replacing the in-line packages (e.g., TO220 with lead inductance of 10-20 nH [32]) with low-inductance packages (e.g., DPAK with a parasitic inductance of 2.5 nH, LGA with a parasitic inductance of 0.2 nH, GaN/px with a parasitic inductance of 0.2 nH [33]) for the primary-side switches;

2) reduce the turn-off gate resistance, increase the current capability of gate driver and/or use wide-bandgap (WBG) switches (e.g., GaN eFET [34] and GaN eHEMT [35]) to enable faster turn-off and lower off-switching losses.

## V. Conclusion

In this paper, a new fixed-frequency PWM controlled structure-reconfigurable SRC is proposed for renewable energy systems. The operation principle and characteristics are analyzed in detail. The experimental results from a 500-W converter prototype are presented to verify the theoretical analysis. The proposed converter is able to deal with a wide input voltage range and to configure its output voltage to be compatible with both the 110/120-V and 220/230/240-V grid voltage levels. The primary switches can achieve ZVS-on and the secondary diodes turn off under ZCS. In addition, the conductions losses do not vary significantly despite the fourfold (from 0.5 to 2) voltage gain range. Therefore, the proposed converter can maintain high efficiencies over a wide voltage gain range.

Nevertheless, the primary switches $S_3$-$S_4$ suffer from a high turn-off current when the converter operates in the middle area of the gain range. Therefore, the precautions of lowering the switching loop inductance and enabling fast turn-off of switches should be taken to reduce the turn-off losses.

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